ABSTRACT OF THE DISCLOSURE

Methods for formal verification of circuits and other finite-state systems are disclosed. Formal definitions and semantics are disclosed for a model of a finite-state system, an assertion graph to express properties for verification, and

5   satisfiability criteria for specification and automated verification of forward implication properties and backward justification properties. A method is also disclosed to compute a simulation relation sequence ending with a simulation relation fixpoint, which can be compared to a consequence labeling for each edge of an assertion graph to verify implication properties and justification

10   properties according to the formal semantics. A method for representing and verifying assertion graphs symbolically is disclosed that provides an effective alternative for verifying families of properties. A symbolic indexing function provides a way of identifying assignments to Boolean variables with particular scalar cases. Formally defining a class of lattice domains based on symbolic

15   indexing functions, provides an efficient symbolic manipulation technique using BDDs. Other methods and techniques are also disclosed herein, which provide for fuller utilization of the claimed subject matter.